

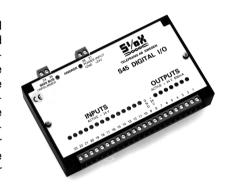
**TELEFRANG AB** 

# **DIGITAL I/O MODULE**

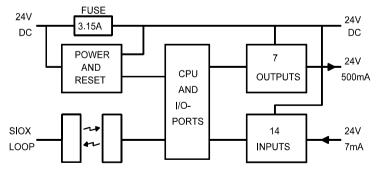
**S45** 

# **General Description**

S45 is a general purpose digital I/O module with 7 sourcing outputs and 14 inputs, all 10 V - 35 V DC. The outputs can supply 0.5 A each and have short circuit protection. Through the built-in CPU, several options are selectable including digitally filtered and edge triggered inputs, pulse counters, increment and absolute (Gray) encoder inputs, watchdog, PLC, etc. The module communicates with the central computer via the opto-isolated SIOX bus.



## **Block Diagram**



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# WARNING-symbol:

refers to the text / diagram on page 6 in the manual read carefully:

3: Separate Power Supplies.

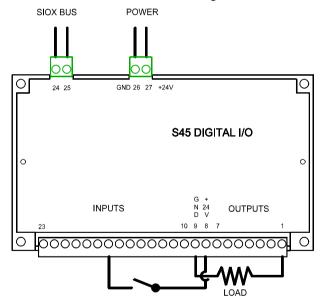


## Installation and Startup

The module is equipped with a 2-terminal power connector, a 2-terminal SIOX bus connector and a 23-terminal I/O connector.

To get the module "up and running" all that has to be done is to connect power to terminals 26 (ground) and 27 (+24 V DC), connect the unpolarized SIOX bus to terminals 24 and 25, and connect relays, pushbuttons, etc. to inputs and outputs.

The SIOX modules should be interconnected through a two-wire, low capacitance twisted pair. Shielded cables may be used but unless a correct strategy for shield grounding is adopted, it may prove to be of little benefit. The total resistance of the bus should not be higher than 2 \* 50  $\Omega$ .



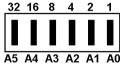
The communication bus is opto-isolated from the rest of the module.

At delivery the module is set up to communicate using address 1, in Data Mode using Single Data and one address. The communication speed is set to 4800 bits/s. General principles for the SIOX bus and communications are described in a separate manual, "SIOX System Description".

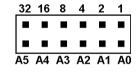


There are two possible ways of defining one of the 63 addresses for an S45 module: either through jumpers located inside the unit or by the internal EEPROM in the module. If any combination of jumpers except all six installed or all six removed is used at power-up, the module will choose this jumper combination as the correct address. The panel has to be removed in order to access the jumpers.

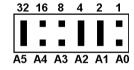
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= 00 : Illegal, will use EEPROM definition. If the EEPROM address is 00 too, Central Mode will be selected at power-up, and the S45 acts as bus master.



= 63 : Illegal, will use EEPROM definition.



= 25: Valid address (16 + 8 + 1 = 25).

The jumper positions A0 - A5 contribute their values 1, 2, 4, 8, 16 and 32 when the corresponding jumper is <u>removed</u>.

All jumpers installed would generate the invalid address 0, and all jumpers removed would be equal to the "reserve" address 63. In this case, the module checks its internal parameter 01 for a valid address number. Should none be found, address 63 will be selected.

The selected address, either from the jumpers or the EEPROM, is finally saved in the RAM parameter 01 and used for all subsequent communications until this parameter is changed or a new power-up is performed.

A special feature is added to help recover "lost" modules, i.e. when an unknown bit rate and/or address is selected or the PLC runs a program that erroneously alters parameters that control the communication. To recover such a module, carry out the following steps:

- 1. Disconnect power.
- 2. Remove all address jumpers except for A0 and A1 but **rotate** the jumpers 90° from their normal position. Please refer to the figure below.



- 3. Apply power. The module will now communicate at 4800 bits/s on address 63 with the PLC and any options disabled.
- 4. Check and reconfigure the module for proper operation.
- 5. Restore correct jumper address.

## **Indicator LEDs**

Two LEDs in the top left of the module indicate SIOX bus status:

The GREEN LED is lit when a bus voltage is applied and flickers a little as communications are sent on the bus. If this LED is dark, the SIOX central and wiring must be checked.

The RED LED is lit each time the module answers to a call to the preset address as described above. If the green LED is on but not the red, check the supply of the module and then the central communications.

# **Power Supply**

The power supply voltage range is 10 - 35 V DC. The power leads must be designed to carry the load current. Recommended minimum area is 0.75 mm<sup>2</sup> (AWG 18). The outputs are protected by an internal 3.15 A, Quick Blow fuse.

The module can be supplied with power in three ways.

1. Via the 2-terminal Power Plug.

Terminals 26 (Ground) and 27 (internally fused). These terminals are connected to the I/O connector at 9 and 8, respectively.

This alternative is generally recommended, since faulty connections to the I/O connector will cause the internal fuse to blow, while power is still supplied to the module's logic.

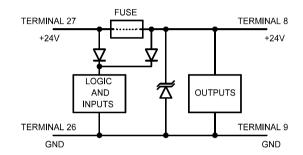
2. Via the 23-terminal I/O Connector.

Terminals 9 (Ground) and 8 (non-fused).

## 3. Separate Power Supplies.

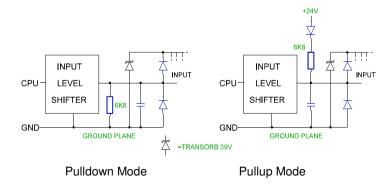
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Power is connected to both 26, 27 and 8, 9. If this is done, the fuse joining 27 and 8 must be removed. Otherwise excessive current will flow between the two power supplies until one of them breaks down or the fuse blows. Separate power supplies are useful, e.g. if the supply at terminal 8 shuts down in case of an emergency. The other supply powering the logic makes it possible for the central computer to communicate with the module and still read input related information.



## Inputs' Hardware

The inputs are either pulled down to ground or pulled up to the power supply voltage. This feature is software controlled, see pages 9 and 15. However, pullup mode should be avoided for supply voltages lower than 18 V DC.



The input is "0" when the input voltage is between -0.5 V to 3.5 V and "1" between 4 V to 35 V.

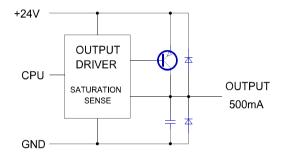
The inputs are protected by capacitors and clamping diodes. Positive and



negative surges are dumped into the module's ground plane, please refer to the figures above. In addition, each input has a capacitor connected to the ground plane. The slew-rate of an input surge is restricted, hereby improving the ability to withstand electrical interference and electrostatic discharges.

# **Outputs Hardware**

The output stage is shown in the following figure.



An output can source a maximum of 500 mA into an external load connected between the output and the ground.

The leakage current in the output transistor causes an unloaded output to float at approximately the same voltage as the power supply.

The short circuit protection is partly implemented in software, sensing the output current every 500  $\mu$ s and turning off overloaded outputs. Overloaded outputs are flagged in a separate register.

When first activated, an output will be left on for a period of  $500~\mu s$ . After this time the output is checked. If at that time the output transistor is still not saturated, the output is regarded as short-circuited and will be deactivated. This short-circuit check cycle is repeated eight times per second until the short is removed, hereby reducing the heat build-up in the output stage to a negligible level.

If the load capacitance is large, it might not be possible to activate the corresponding output because the output stage will not have enough time to charge the capacitance before short-circuit is checked. Typically, a load capacitance of minimum 5  $\mu F$  is acceptable which is far beyond the capacitance values for normal loads found in industrial installations.

Inductive loads will turn on properly but at turn-off the energy stored in the inductor will discharge through the built-in clamping diodes. Local back diodes



directly across the loads are recommended to reduce induced voltage surges in the connecting cables.

## I/O Functions

The module includes a microprocessor that controls communication and preprocesses information. This CPU checks and controls all inputs and outputs regularly according to control parameters in various registers. Results, such as detection of overloaded outputs and number of inactive to active transitions on inputs, are stored in other registers accessible by the central computer. In this way the central computer is relieved of trivial and communication-intensive tasks.

The table below summarizes the input connections for different configurations. Inputs are designated I and counters C. Gray code bits are designated B. Increment encoder inputs are designated EnX, EnY and EnZ.

TERM. NO.		23	22	21	20	19	18	17	16	15	14	13	12	11	10
INPUT NO.		114	l13	l12	111	l10	19	18	17	16	15	<b>I</b> 4	13	12	11
INTERLOC	K								YES	YES	YES	YES	YES	YES	YES
GRAYCOD	E	MSB	B12	B11	B10	В9	B8	В7	B6	B5	B4	ВЗ	B2	B1	LSB
COUNTER	S	C14	C13	C12	C11	C10	C9	C8							
ENCODER	S	·	EnZ	EnZ	EnY	EnY	EnX	EnX							

Input edge triggering and debounce are available on inputs I1 - I14. The only exception is the fast counter, which has no debounce at all. The debounce time also affects the maximum count frequency of counters C8 - C13. However, Gray coding and incremental encoder processing uses un-debounced input data.

#### **Available Functions:**

#### Inversion of Inputs

Each input can be set individually to invert input data. Because of this, the terms inactive and active are used instead of high and low, 1 and 0, etc. In the normal non-inverted mode an inactive input is 0 V - 3.5 V and an active one 4 V - 35 V. In inverted mode an input is inactive for voltages 4 V - 35 V and active for 0 V - 3.5 V. Parameter 0C controls input inversion.

### Pullup/Pulldown on Inputs

F

This feature selects pulldown or pullup at inputs. It is common to all inputs and cannot be set individually. The flag bit to control this feature is located in parameter  $\emptyset$ 1. However, pullup mode should be avoided for supply voltages lower than 18 V DC.

## Debounce on Inputs

The debounce time can be set in 4 ms increments in the lower half of parameter 3. Maximum debounce time is 1020 ms (hex FF). This setting is common to all inputs I1 - I14 and pulse counters C8 - C13 except the fast counter C14. Please note that Gray code and incremental encoder processing uses input data that is **not** debounced.

### **Edge Triggered Inputs**

Each input can be set individually to register an inactive to active transition. This event is stored in the module and is transmitted to the central computer at the next communication. If that communication is successful, the event is cleared in the module's storage. This feature is controlled by parameter 0A.

Please note: If this feature is used with the automatically communicating SIOX protocol the AUTO OFF feature should be used. This is necessary in order to give slow application software in the central computer time to process the data before the next communication clears the event from storage.

## Counters

There are six 16-bit pulse counters incrementing on each inactive to active transition of the input with the same number (C8 - C13). The maximum counting speed is 1000 Hz for a symmetrical square wave or as determined by the input debounce time. These counters may be preset by writing to them.

For special purposes, the remaining inputs I1 - I6 and I14 can be set to count in a similar way by setting the Option 000A in parameter 02. The normal Incremental and Gray code handlers will then be disabled, and pulses on inputs cause parameter 0B to count as C1, parameter 0D as C2, parameter 0E as C3, parameter 0F as C4 and parameters 20 - 22 as C5, C6 and C14, respectively.

#### **Fast Counter**

This counter, connected to input 14, is 32 bits long, using two 16-bit parameters, 1E (most significant) and 1F (least significant). There is no debounce available, the maximum counting frequency being 20 kHz. This counter always counts up on low to high transitions, and is not affected by input inversions. The low 16 bits can be used as a prescaler by presetting parameter

1F to 1 - 65535 (1 - hex FFFF). When reaching the prescale value it resets, incrementing the high 16-bit parameter 1E. A prescale value of 0 selects a continuous 32-bit counter.

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The high 16 bits of the counter can be read or written, while the low 16 bits can only be read. A write to parameter 1F just changes the prescaler without presetting the counter. The prescaler cannot be read.

#### Example:

Setting the prescaler to 100 (hex 64) lets the high 16 bits to be incremented once per 100 input edges.

Since it is impossible to read all 32 bits in one communication, carry from the low 16 bits may occur between communications. Therefore, at each read of the first, most significant parameter, the second parameter will be internally buffered and read out in a directly following communication. The counter may continue counting meanwhile. This fast counter works independent of the 16-bit optional C14 counter option described above.

Please note: If data mode is used in accessing this counter and the maximum readable count length of 28 bits is desired, the prescaler should be set to 16384 (hex 4000).

## **Gray Code Conversion**

The module can be connected to an absolute encoder that employs Gray code. It can convert Gray code to ordinary binary code. This is done by setting as many bits in the Gray code mask register (parameter ØB) as there are in the encoder. The result is shown in the binary code register in parameter ØD. The least significant bit of the encoder must be connected to I1. Further bits must be allocated consecutively, in ascending order.

#### Incremental Encoder Counters

Three 16-bit up/down counters can handle the signals from rotary encoders. They are designated EnX, EnY and EnZ and use inputs I8/I9, I10/I11 and I12/I13, respectively. One count is registered on each transition of either input, incrementing when the phase of the higher input number leads that of the lower number.

The maximum counting speed is limited by the internal sampling rate of the inputs which is 0.5 ms. This means that any two transitions must be separated by at least 0.5 ms in order to be properly recognized.

#### Interlock Registers



communication are deactivated until the next successful communication. When the timer is cleared, the watchdog has no effect on the outputs.

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The module may inhibit particular outputs when various inputs are inactive. For this purpose, seven definition registers exist, one for each of the inputs I1 - I7. Setting one or more bits in such a register inhibits one or more of the outputs when the input is inactive. Response time is limited only by the debounce time and not by the central computer response time. When all bits of the interlock registers are cleared, none of the inputs affect any output. The contents of all interlock registers whose inputs are inactive are OR:ed together and the result placed in the interlock inhibit sum register.

The interlock function has higher priority than the PLC so that emergency stops are always granted.

Please note: The edge trigger function must not be enabled on inputs used for interlock. This is because a "glitch" sets the input register bit active, thus fooling the interlock function to believe that the input is active.

These 8-bit registers are located in pairs I1:I2, I3:I4 and I5:I6 in parameters 4 -6. The register for I7 is located together with the interlock sum register in parameter 7.

#### Example:

Assume that the interlock register contains the bits 00000110 for I1 and 00000011 for I2. All other interlock registers are zero. If both I1 and I2 are active the result in the interlock inhibit register would be 00000000, i.e. no outputs would be inhibited. If I2 becomes inactive the interlock inhibit detect register would contain 00000011. If I1 also becomes inactive this register would contain 00000111. If I2 then becomes active it would contain 00000110.

#### Overload Detection

A seven-bit register shows which of the activated outputs that are currently overloaded. It is paired with the output register in parameter 8 and is not affected by a write to this parameter.

#### Output Register

The seven least significant bits of parameter 8 controls the outputs. The eighth bit may be used by the PLC, if enabled.

## Communication Watchdog

This feature consists of a timer located in the high half of parameter 3. The timer can be preset in 0.25 s increments and is restarted each time a successful communication with the module is carried out. If communication ceases for longer than the preset time (max 65 s), outputs controlled by the

## **Slave Communications**

The S45 module communicates as a slave using various message types defined in the manual "SIOX System Description".

1. Data Mode Message. One Address, Single Data.

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In receiving this message type, S45 behaves as a basic I/O module with 14 inputs and 7 outputs. The data transmitted to the module controls the outputs, while the answer contains the current state of the inputs.

2. Data Mode Message. Two Addresses, Single Data.

For this message type the first address has the same properties as in a Single Address module. Data at the second address selects which internal parameter value to send in reply. However, it is only possible to answer with 14 of the 16 parameter bits. This mode is available only if enabled in the internal RAM/ EEPROM. Please refer to page 19. Data Mode Access to Parameters.

3. Data Mode Message. One Address, Double Data.

For this message type the module receives two data bytes in each communication. The first is used as data to control the outputs and the second as an address to select which internal parameter value to send in reply. This mode is available only if enabled in the internal RAM/EEPROM.

It is possible but pointless to select both Double Data Mode and two addresses on a module. Fither mode should be used.

4. String Setup Mode. One Address.

This message type is used to read or change one configuration parameter in RAM or EEPROM. All internal parameters can be read or written.

5. String Text Mode message. One Address.

The module can receive text messages, but these can only be emptied and interpreted by a PLC program in the S45. Such a program can also prepare text answers, e.g. containing condensed I/O statistics. If none is prepared, the text answer will be empty.



## **Communication Options**

Some bits, located in parameters 00 and 01 in the module, control communication modes...

Restart of the module is accomplished by writing hex FFFF to parameter 00. For example, to change the bit rate of a remote S45, first write the corresponding code into EEPROM parameter 00, then write hex FFFF to the same parameter (in EEPROM or RAM). The module will now restart and commence communication on the new bit rate.

<u>Disable String Text Output</u> causes text calls to be interpreted as were they string setup calls (for compatibility with older modules).

<u>Disable Data Mode Output</u> disables the possibility to control outputs in Data Mode, reducing the risk of inadvertently changing outputs as a result of a communication error.

<u>Double Data Mode Safeguard</u> enhances the integrity of Data Mode. If this function is active, the data controlling the outputs must be the same for two communications in a row to change the outputs.

Communication Speed can be set to the bit rates 300, 600, 1200, 2400, 4800, 9600 or 19200 bps in parameter 00. Note, that a change must be carried out in EEPROM and the module restarted for the new speed to become effective.

Automatic Bit Rate Selection allows the module to automatically identify and select the communication speeds 1200, 2400, 4800, 9600 and 19200 bps. It is allowed by selecting 0 in bits 11...8 in parameter 00. When only a single rate will be used or when the rates 300 or 600 are required, the code for that speed should be set in bits 11...8. Note also that some short messages at 19200 bps may be difficult to identify if the S45 is currently running at 1200 bps, since the whole message may appear shorter than a single character. This will not be a problem for a normal mix of messages.

#### PLC, Spy and Master Mode Capabilities

Please refer to the "SIOX PROGRAMMABLE CONTROLLER" manual.

## RTC, Real Time Clock

Parameter 17 contains a real-time clock, incrementing each second. The last 8 bits of parameter 16 increments each 10 ms to create a real-time clock. When it reaches the value 100 (hex 63) it is cleared and the 16-bit register in parameter 17 is incremented to act as a seconds counter. No battery backup, however, is possible for the RTC, only for the entire S45.



Any of the PLC instructions DATE (DATM...DATS) changes, when first run, parameter 17 from a 65536 seconds counter to a minutes + seconds register with a maximum value of hex 3B3B (59 minutes, 59 seconds).

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This software controlled RTC depends on the internal CPU clock for accuracy. To optimise its speed, the first half of parameter 16 can be increased or decreased a few steps (in EEPROM for permanency). Alternatively the RTC parameter 17 may be rewritten (in RAM) at any time, which also restarts the 10ms counter (second half of parameter 16).

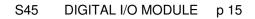
## **Parameter Description**

1024 configuration parameters (2048 bytes) for the S45 are stored in an internal EEPROM. At power-up the first 256 parameters (512 bytes) of EEPROM data are transferred to RAM. 256 bytes are reserved as PLC program space (parameters hex 80 - FF). The remaining 768 parameters (1536 bytes) are available for PLC program overlays, data logging, texts and nonvolatile storage for PLC applications. Features are typically active when a parameter is set to a non-zero value.

Working modes may be changed in RAM when needed but will be lost after a power down unless saved in EEPROM. Writing to an EEPROM parameter will also save the data in RAM.

The simplest way to access all parameters is to use the MEMSETUP menu in the SIOXUSER or Visual Setup programs on a PC or equivalent.

Below follows the default values and a description of each parameter. All parameter values are shown in hexadecimal notation.



<u>Parameter</u>	Factory Default	Function
ØØ	2701	Control bits and bit rate
Ø1	0100	Address and control bits
02	0000	Customer options and PLC spy address
<b>Ø</b> 3	0000	Timeouts and debounce time
04	0000	Interlock mask I1 and I2
<b>Ø</b> 5	0000	Interlock mask I3 and I4
<b>Ø</b> 6	0000	Interlock mask I5 and I6
07	0000	Interlock mask I7 and inhibit register
08	0000	Overload and output register
<b>Ø</b> 9		Input register
ØA	0000	Edge trigger control
ØВ	0000	Gray code mask
ØC	0000	Input inversion mask
ØD	0000	Binary converted Gray code
ØE	0000	Inc. encoder X
ØF	0000	Inc. encoder Y
10	0000	Inc. encoder Z
11	0000	PLC controlled outputs/program counter
12	0000	PLC timebase and run flags
13	0000	PLC status flags
14	0000	PLC 16 bit V accumulator
15	0000	PLC 16 bit timer
16	0000	RTC most significant word
17	0000	RTC least significant word
18	0000	Counter C8
19	0000	Counter C9
1A	0000	Counter C10
1B	0000	Counter C11
1C	0000	Counter C12
1D	0000	Counter C13
1E	0000	Counter C14 most significant word
1F	0000	Counter C14 least significant word
20-3F	0000	Free for PLC use
40-7F	0000	Spy/Master Mode configurations
80-3FF	0000	PLC storage/program area



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# **Parameter Specifics**

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	-	
<u>Parameter</u>	<u>Data</u>	<u>Function</u>
00	8xxx 4xxx 2xxx 1xxx xNxx  xxxN	Permit write to <u>all</u> parameters. Otherwise internal system memory areas are write protected. Converts String Text Mode to String Setup. Disables Data Mode outputs control. Enables Double-byte Data Mode. Bit rate. Must be changed in EEPROM followed by a restart of the unit in order to have effect. $N = 0 = \text{Automatic } 1200 - 19200 \text{ bps}$ $N = 3 = \text{300 bps}$ $N = 4 = \text{600 bps}$ $N = 5 = \text{1200 bps}$ $N = 6 = \text{2400 bps}$ $N = 7 = \text{4800 bps}$ $N = 8 = \text{9600 bps}$ $N = 9 = \text{19200 bps}$ $Number of permitted addresses. In this module N may be 1 or 2. The module is restarted by writing hex FFFF.$
01	NNxx 8xxx xx8x xx1x xxx2	01 - 3F = first address of module.  Please note that if the number of permitted addresses is two, the address range is reduced to 01 - 3E.  Master Flag starting communications defined in parameters 40 - 7F.  Spy Inhibit. Spy area will be free for general use.  0 = inputs pulldown, 1 = inputs pullup  Enables double communication safeguard. When set, two identical Data Mode communications must be carried out before the digital outputs can change.
02	0000	Options for customer specific functions.
03	TTxx	Timeout to clearing outputs if communication stops. TT = 00 = no timeout. $TT = 01  to FF = timeout  250  ms - 65  s.$ Inputs debounce time. $DD = 00 = no debounce, i.e. 1 ms.$ $DD = 01  to FF is debounce time in 4 ms steps.$

<u>Parameter</u>	<u>Data</u>	<u>Function</u>
<b>Q4</b> MMxx		Input I1 interlock mask  MM = 00 - 7F is a bit pattern where D0 (LS bit) affects output Q1, D1 affects Q2, up to D6 which affects Q7.  0 signifies that the corresponding output is independent of input I1. 1 signifies that the respective output can be set <i>only</i> if I1 is active.
	xxMM	Input I2 interlock mask.
05	MMxx xxMM	Input I3 interlock mask. Input I4 interlock mask.
<b>0</b> 6	MMxx xxMM	Input I5 interlock mask. Input I6 interlock mask.
07	MMxx xx I I	Input I7 interlock mask. Shows the outputs that are inhibited by inputs.
08	CCxx xxOO	Shows active, overloaded outputs; read only. Output register, controls which outputs that are switched on.
09	1111	Debounced inputs I14 - I1, read only.
0A	BBBB	Edge trigger enable bits for inputs.
<b>0</b> B	GGGG	Gray code mask.
0C	1111	Input inversion mask.  Ø = do not invert input data.  1 = invert input data.
0D	BBBB	Gray code converted to binary, read only.
0E	EncX	Incremental encoder counter X, 16 bits, DI8 / 9.
<b>0F</b>	EncY	Incremental encoder counter Y, 16 bits, DI10 / 11.
10	EncZ	Incremental encoder counter Z, 16 bits, DI12 / I13.



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<u>Parameter</u>	<u>Data</u>	<u>Function</u>
11	PPxx	00 - 7F = PLC controlled outputs. PP is a bit pattern where D0 (LS bit) corresponds to output Q1, D1 to Q2, D6 to Q7. 0 signifies that the output is controlled by the ordinary SIOX communication. 1 signifies that the PLC controls the output. 00 - FF = PLC program counter.
12	TTxx  xx4x xx1x	00 - FF = PLC timer tick size. 00 = 1/16 s. 01 - FF = TT/1024 s. 40 gives the same time as 00. EEPSH remapping of EEPROM active. PLC single step.
	xx2x xxx1-8	<ul> <li>Ø = continuous run.</li> <li>1 = single step.</li> <li>Singlestep done.</li> <li>PLC run bits.</li> <li>Ø = stop.</li> <li>1-8 = active task.</li> </ul>
13	x8xx x4xx x1xx xx2x xx1x xxx1	If set, clears the PLC edge inputs register, will be cleared automatically.  Outputs Watchdog flag. For PLC use.  0 = watchdog not triggered.  1 = watchdog triggered due to lacking comm.  Valid communication with module.  PLC overflow flag L.  PLC carry flag C.  PLC bit accumulator A.
14	VVVV	PLC V accumulator, 8000 - 7FFF = -32768 - +32767.
15	TTTT	PLC T timer, 0000 - FFFF. Tick rate is defined in parameter 12.
16	80xx-14xx	Real Time Clock fine tuning. 00xx = no adjustment.
	xx00-xxx63	Real Time Clock 10 ms counter, reset at 99*10 ms.
17	0000-FFFF	Real Time Clock seconds counter.



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Parameter	<u>Data</u>	<u>Function</u>
18	CCCC	C8 counter, 16 bits. All counters C8 to C13 may be preset. If the preset value is written in EEPROM the counter will be set to this value at power up.
19	CCCC	C9 counter, 16 bits.
1 <b>A</b>	CCCC	C10 counter, 16 bits.
1B	CCCC	C11 counter, 16 bits.
1C	CCCC	C12 counter, 16 bits.
1D	CCCC	C13 counter, 16 bits.
1E	CCCC	Fast Counter, most significant 16 bits.
1F	CCCC	Fast Counter, least significant 16 bits; write: 0001 - FFFF = prescale with 1 - 65535. 0000 = prescale with 65536.
20 - 3F	NNNN	Free for PLC use (byte addresses 40 - 7F).
40 - 7F	SSSS	Spy/Master Mode configurations (byte addresses 80 - FF). Free for PLC use if the Spy Inhibit bit in parameter 01 is set.
80 - FF	PPPP	PLC program space (byte addresses 100 - 1FF).
100 - 3FF	PPPP	PLC Program/Application Area, these para-meters are not automatically copied from EEPROM to RAM at power-up. RAM values are protected from inadvertent changes, while EEPROM data is freely usable for PLC data logging, texts or program overlays (byte addresses 200 - 7FF).

For further information about the PLC, Spy and Master Modes, please refer to the "SIOX PROGRAMMABLE CONTROLLER" manual.



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#### **Data Mode Access to Parameters**

S45

In addition to String Mode setup communication, parameters can be accessed in Data Mode. For this purpose, the seven extra control bits from the central computer in Double Data Mode, or data at a possible second address are used. These extra bits are used as a selector number to indicate which parameter in RAM or EEPROM is to be returned. Since only 14 data bits can be returned, the two most significant bits of the internal registers are not accessible in Data Mode. Further, it is impossible to write data to a parameter using Data Mode, except to clear some RAM parameters.

To permit Data Mode access to parameters, the control bit for Double Data Mode must be active or the number of addresses must be set to  $\emptyset 2$ .

The selector number consists of seven bits:

#### CAAAAAA

C = control bit, AAAAAA = parameter address in the 00 - 3F range.

 $C = \emptyset$  = read RAM contents at address AAAAAA.

C = 1 = return RAM contents at address AAAAAA and clear.

It should be noted that, although only 14 bits can be read from an address, all 16 bits will be cleared.

At addresses 00 - 07, 09, 0A and 0C it is not possible to clear the RAM since this would disrupt the operation of the module. Changes to these parameters should be carried out using the string setup mode.



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## Example 1:

Assume that the module has address one (1) and uses double data mode. The content of counter C9 is 0007. To read counter C9 and set outputs Q1 and Q2 the following message will be sent.

5 Byte #

Message from

central computer: 03 19

Answer from module: 07 00

Byte 1 is the module's data mode address, byte 2 is output data to set Q2 and Q1 and byte 3 is the parameter number. Byte 4 is LSB and byte 5 is MSB of counter C9.

## Example 2:

Assume that the module has address one (1) and uses two addresses. To read counter C9 the following message will be sent.

Byte # 2 4

Message from

central computer: C2 19

Answer from module: 07 00

Byte 1 is the module's address (the second address), byte 2 is the parameter number. Byte 3 is LSB and byte 4 is MSB of counter C9.

The characters in **bold** in the two examples are the actual characters transmitted on the SIOX bus.



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# Electrical Specifications (T<sub>amb</sub> = 20 °C)

- 4	-			
	Min	Тур	Max	Unit
Power Supply Voltage Power Supply Current (Outputs off, inputs pulldown)	10 10	24 16	35 20	V mA
Input Voltage Range High-level Input Voltage Low-level Input Voltage Input Current (Vin = 24 V DC)	-0.5 4	24 7	35 3.5	V V V mA
Output Saturation Voltage			0.3	٧
Output Current Output Short Circuit Current	500		500 1300	mA mA
Output Off Leakage Current (V <sub>supply</sub> = 24 V DC)			500	μΑ
SIOX Current (no Communication)		0.9	1	mA
Maximum square wave count frequency C8 - C13 Fast Counter			1 20	kHz kHz
<b>Environmental Specifications</b>				
Operating Temperature Range	0		+55	°C
Storage Temperature Range	-40		+85	℃
Mechanical Specifications				
Dimensions (excluding 35 mm DIN clip)	140	) x 81 x 25	5	mm
Weight		230		g

Removable connection blocks with screw terminals are PHOENIX contact type MSTB. Maximum wire area is 2.5 mm<sup>2</sup> (AWG 12).

# Assistance

on safety and technical matters is available from:

TELEFRANG AB Victor Hasselblads Gata 9 S-421 31 V FRÖLUNDA SWEDEN

Tel: +46 31 40 30 60 Fax: +46 31 40 20 25 E-mail: info @telefrang.se